PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Lap Wai Chow, et al.	Examiner: Nguyen, Joseph H. Art Unit: 2815
Patent Appln: 09/768,904	Our Ref: B-3964 618029-8
Filed: January 24, 2001	Date: November 12, 2004
For: "INTEGRATED CIRCUITS PROTECTED AGAINST REVERSE ENGINEERING AND METHOD FOR FABRICATING THE SAME USING AS APPARENT METAL CONTACT LINE TERMINATING ON FIELD OXIDE"	Re: AFFIDAVIT

AFFIDAVIT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Declaration of Joseph Jensen

1. My name is Joseph Jensen.

2. I am a principal research scientist and the department head at HRL Laboratories for the microelectronics lab.

3. I received my B.S. degree in Electrical Engineering in 1980 from the University of California at Los Angeles and my M.S. also in Electrical Engineering from the same university in 1983.

4. My professional history, patents, publications and honors are listing in the attachment hereto.

5. I have reviewed independent claims 9 and 13 pending in the above-identified application. Both of these claims include the recitation "wherein said plug metal contact is electrically isolated from said contact region." I have also reviewed the Examiner's Advisory Action dated September 29, 2004 in which the Examiner asserts that those words are equivalent to "not shorted."

6. Based upon my experience, training and education as a professional engineer and my understanding of the electrical arts, I believe that the Examiner is utterly incorrect in making the assertions that he makes in the Advisory Action referred to above.

7. The Examiner uses a simplistic direct current (DC) analysis when taking the position that a gate of an FET device is electrically isolated from its associated drain. At DC, the resistance may well be infinite. However, since FET devices are normally used in alternating current applications, those skilled in the art know, indeed, that FET devices can and will respond to the signals provided at the gates thereof. As such, the gates are hardly "electrically isolated" from the rest of the structure of the device, be it the drain or the source, as asserted by the Examiner. The impedance is anything but infinite. So, while there may be no DC "short" between a gate and either the source or drain of an FET transistor, that does not imply that the gate is electrically isolated from either the drain or the source. Indeed, that which happens on the gate directly influences that which happens at the source and drain of a FET device and therefore the gate of a FET device is not electrically isolated from either its source or its drain.

8. The assertions of the Examiner to the contrary in the Advisory Action dated September 29, 2004 are utterly incorrect. In simple terms, "not shorted" is a sufficient but not necessary condition for "electrically isolated."

9. Further declarant sayeth not.

DECLARATION

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Joseph Jensen

Nov 12 2004
Date